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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/808,793

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Ervin T. Hill

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08/02/2005

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EXAMINER

YEVSIKOV, VICTOR V

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/808,793

Applicant(s)

HILL ET AL.

Examiner

Victor V. Yevšikov

Art Unit

2891

AM

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/24/04
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 7-9 rejected under 35 U.S.C. 102(a) as being anticipated by Chao et al. (US 2005/0098821 A1).

With respect to claims 1 Chao teaches a method for lithography patterning of the thin film stacks, comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer 106, 113 and an oxide layer 104, 111;

forming a hardmask layer 114, 115 comprised an anti-reflective coating (ARC) layer (§ 0026) on the thin film stack;

patterning the ARC layer (figs. 6,7);

etching the hardmask layer using the patterned ARC layer as a mask (fig. 6); and etching the thin film stack using the hardmask layer as a mask (figs. 9, 10).

With respect to claims 5, 6, 8 and 9 Chao teaches a method wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etches chemistries.

the hardmask layer comprises amorphous carbon.

ARC layer is removed during the etching of the thin film stack.

removing the hardmask material from the thin film stack.

With respect to claims 10 Chao teaches a method for lithography patterning of the thin film stacks, comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer 106, 113 and an oxide layer 104, 111;

forming a hardmask layer 114, 115 comprised an anti-reflective coating (ARC) layer (§ 0026) on the thin film stack;

patterning the ARC layer (figs. 6,7);

etching the hardmask layer using the patterned ARC layer as a mask (fig. 6); and etching the flash memory gate stack using the hardmask layer as a mask (figs. 9, 10).

With respect to claims 5, 6, 8 and 9 Chao teaches a method wherein

the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etches chemistries (§0026);

the hardmask layer comprises amorphous carbon (§0026);

ARC layer is removed during the etching of the thin film stack (fig.10).

removing the hardmask material from the thin film stack.

With respect to claims 10 Chao teaches a method for lithography patterning of the thin film stacks, comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer 106, 113 and an oxide layer 104, 111;

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forming a hardmask layer 114, 115 comprised an anti-reflective coating (ARC) layer (§ 0026) on the thin film stack;

patterning the ARC layer (figs. 6,7);

etching the hardmask layer using the patterned ARC layer as a mask (fig. 6); and etching the flash memory gate stack using the hardmask layer as a mask (figs. 9, 10).

With respect to claims 13, 15, 16, 18 and 19 Chao teaches a method wherein: the flash memory gate stack is comprised of a gate dielectric layer 104, a floating gate layer 111, an inter-electrode dielectric layer 112, and a control gate electrode layer 113;

the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etches chemistries (§0026);

the hardmask layer comprises amorphous carbon (§0026);

the ARC layer is removed during the etching of the flash memory gate stack and removing the hardmask material from the flash memory gate stack (fig.10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 —4, 11, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Mahorowala et al. (US 6,869,899 B2).

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Chao discloses the features out lined above, but does not show exactly a method wherein the ARC layer is patterned with resist using 193 nm or less lithography; the thickness of the resist is less than 5000 Å; and the hardmask layer has a thickness of between 1000 and 3000 Å and the ARC layer has a thickness of between 100 and 500 Å.

However, Mahorowala teach the method wherein the ARC layer is patterned with resist using 193 nm or less lithography; the thickness of the resist is less than 5000 Å; and the hardmask layer has a thickness of between 1000 and 3000 Å and the ARC layer has a thickness of between 100 and 500 Å (reference: figs. 1B, 2A with corresponding text; col. 1, lines 16-39; col. 2, lines 40-49; cl. 18).

It would have been obvious to those skilled in the art using 193 nm lithography and resist, hardmask and ARC layers as taught by Chao / Mahorowala for provides method for producing a lithographically printed image having a reduced critical dimension.

Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Kumar et al. (US 2005/0079706 A1).

Chao discloses the features out lined above, but does not show exactly a method wherein the hardmask layer comprises Applied Materials film.

However, Kumar teach the method wherein the hardmask layer comprises Applied Materials film (§0041).

It would have been obvious to those skilled in the art using Applied Materials film as taught by Chao / Kumar for provides method for reduced critical dimension.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, William B. Baumeister, can be reached on (571) 272-1722. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2891

July 29, 2005

David Zarneke
DAVID ZARNEKE
PRIMARY EXAMINER
7/29/05